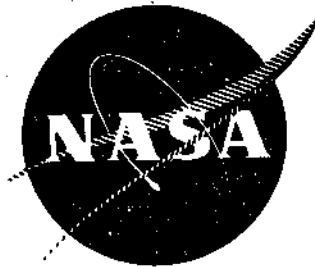


PP
NASA CR-121021



DESIGN AND FABRICATION OF WRAPAROUND
CONTACT SILICON SOLAR CELLS

(NASA-CR-121021) DESIGN AND FABRICATION
OF WRAPAROUND CONTACT SILICON SOLAR CELLS
J.A. Scott-Monck, et al (Heliotek) - Nov.
1972 30 p CSCL 10A

N73-13051

G3/03 Unclass
50260

by J. A. Scott-Monck, P. M. Stella, and J. E. Avery

HELIOTEK, DIVISION OF TEXTRON INC.

PRICES SUBJECT TO CHANGE

prepared for

Reproduced by
NATIONAL TECHNICAL
INFORMATION SERVICE
U.S. Department of Commerce
Springfield VA 22151

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

NASA Lewis Research Center

Contract NAS 3-15344

1. Report No. NASA CR-121021		2. Government Accession No.		3. Recipient's Catalog No.	
4. Title and Subtitle DESIGN AND FABRICATION OF WRAPAROUND CONTACT SILICON SOLAR CELLS				5. Report Date November , 1972	
				6. Performing Organization Code	
7. Author(s) J. A. Scott-Monck, P. M. Stella and J. E. Avery				8. Performing Organization Report No.	
9. Performing Organization Name and Address Heliotek, Division of Textron Inc. Sylmar, California				10. Work Unit No. 113-33-11-K4357	
				11. Contract or Grant No. NAS3-15344	
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Washington, D. C. 20546				13. Type of Report and Period Covered Contractor Report	
				14. Sponsoring Agency Code	
15. Supplementary Notes Project Manager, John H. Lamneck, Energy Conversion and Materials Science Division, NASA Lewis Research Center, Cleveland, Ohio					
16. Abstract Both dielectric insulation and etched junction contact techniques were evaluated for use in wraparound contact cell fabrication. Since a suitable process for depositing the dielectrics was not achieved, the latter approach was taken. The relationship between loss of back contact and power degradation due to increased series resistance was established and used to design a simple contact configuration for 10 ohm-cm etched wraparound junction contact N/P cells. A slightly deeper junction significantly improved cell curve shape and the associated loss of current was regained by using thinner contact grid fingers. One thousand cells with AMO (135.3 mW/cm ²) efficiencies greater than 10.5% were fabricated to demonstrate the process.					
17. Key Words (Suggested by Author(s)) Silicon Solar Cells Wraparound Contacts			18. Distribution Statement Unclassified - Unlimited		
19. Security Classif. (of this report) Unclassified		20. Security Classif. (of this page) Unclassified		21. No. of Pages 21 30	

* For sale by the National Technical Information Service, Springfield, Virginia 22151

Table of Contents

	Page
I SUMMARY	1
II INTRODUCTION	2
III WRAPAROUND CONTACT	2
A. Effect of Back Contact Removal	3
B. Insulated Wraparound Contact	4
C. Wraparound Junction Contact	9
IV CELL FABRICATION	11
A. Blank Preparation	11
B. Diffusion	11
C. Masking and Etching.	16
D. Contacts	16
E. Sintering and Antireflection Coating	19
V TESTING AND EVALUATION	19
A. Mechanical Integrity	19
B. Electrical Test	19
C. Series Resistance	20
D. Shunt Resistance	20
VI DISCUSSION	20
VII RECOMMENDATIONS	27

LIST OF ILLUSTRATIONS

Figure		Page
1	Effect of Edge Strip Removal on Cell Series Resistance and Maximum Power	5
2	Effect of Center Strip Removal on Cell Series Resistance and Maximum Power	6
3	Wraparound Contact Solar Cells	10
4	Back Contact Design	12
5	Wafer Preparation Flow Chart	13
6	Cell Edge Damage	14
7	I-V Curve of Initial Wraparound Cell	15
8	Edge Evaporation Tooling	17
9	Contact Masks	18
10	Efficiency Distribution for Wraparound Cells	21
11	Short Circuit Current Distribution for Wraparound Cells	22
12	I-V Curves Showing Efficiency Extremes for Wraparound Cells	23
13	I-V Curves of Representative Wraparound Cells (I)	24
14	I-V Curves of Representative Wraparound Cells (II)	25

I. SUMMARY

The purpose of this program was to develop inexpensive and reproducible wraparound contacts which could be used on space quality cells. Two methods were evaluated, an insulated contact using evaporated dielectrics and a wraparound junction contact.

Two dielectrics, SiO_2 and Al_2O_3 , showed promise as insulating materials, but neither could be deposited in sufficiently thin pinhole free layers to be practical. The junction wraparound contact approach was therefore employed to produce 1000 N/P 2×2 cm cells (10 ohm cm).

The relationship between series resistance and rear contact coverage was verified and based on these results a contact configuration was designed to optimize cell output while staying within the constraints of present masking technology. It was necessary to incorporate new handling techniques and modify the wafer preparation schedule to ensure that a rounded and undamaged wraparound contact edge was formed.

A trade-off was made between junction depth and cell curve shape in order to obtain high efficiency wraparound cells. By using a slightly deeper junction and compensating for the loss in current by reducing grid-line width it was possible to produce cells with AMO (135.3 mW/cm^2) efficiencies between 10.5 and 11.6 percent, using an active area of 4.0 cm^2 .

II. INTRODUCTION

The purpose of this program was to develop inexpensive and reliable wraparound contacts which can be used on space quality cells. This program was broken into three tasks, the first being to provide an optimized wrap-around contact configuration. Once this was accomplished, prototype cells were fabricated in order to check the processing procedures, and then a limited production run of 1000 cells was made to prove the manufacturing feasibility. In brief, a wraparound solar cell is a device which has both the diffused and bulk area contacts located on one side. This may be accomplished in a number of ways such as extending the diffused region to the back of the cell or employing isolation techniques that shield the oppositely charged conduction regions from each other.

Historically, the first solar cells built employed wraparound contacts⁽¹⁾, but in order to reduce series resistance separate front and back contacts were developed. As the understanding of photovoltaic theory advanced and the reasons for higher than normal series resistance in wrap-around contacted cells became known, Heliotek re-evaluated this configuration in the mid-sixties. The study showed that loss of contact area on the back of the wraparound cell was responsible for the increased series resistance and that it was possible to conserve enough back area to fabricate a cell that exhibited performance comparable to the conventional device.

The emphasis on low cost arrays developing power outputs in the multikilowatt range has made the wraparound cell more attractive to array designers for many reasons. With present cells the laydown cost is nearly equivalent to the cell cost. Wraparound cells, by confining all contacting to one surface of the cell could reduce laydown cost substantially, as well as provide greater interconnection reliability due to simplified interconnector patterns. The fact that the front surface is free of interconnect bars allows improved array cell packing as well as improved cell radiation protection due to complete coverage of the cell front surface with a protective quartz layer. There is another advantage that has yet to be completely exploited, namely additional output power due to an increase in front surface active area. Before any of these benefits can be realized it is necessary to have a thorough understanding of wraparound contact theory and the ability to translate this knowledge into a processing schedule that yields cells which are competitive with present devices in terms of efficiency and cost.

III. WRAPAROUND CONTACT

There were two approaches considered in the evaluation of an optimum wraparound contact; an etched design with a wraparound junction and an insulated wraparound design. The first approach had already been demonstrated by Heliotek⁽²⁾ while the alternate technique represents a potential improvement, not yet demonstrated, in wraparound contact technology.

The etched wraparound junction contact is formed by first diffusing the entire surface of the silicon blank, then removing, by etching, a portion of the cell back and three of the edges to expose the original material. Thus the P-N junction remains on the top, one edge, and part of the rear surface of the cell. Contacts are deposited such that the grid lines on the active (front) surface continue around the junction edge of the cell to the diffused region on the back of the cell. Electrical isolation is achieved by carefully masking the etched region between the P and N regions prior to contact evaporation. As will be explained in Section IIIA this technique can lead to an increase in series resistance thus reducing the power output of the cell.

To avoid this problem the insulated wraparound contact was proposed. Using this design the N and P regions are formed in the same manner as the conventional cell. Furthermore, the base contact is formed in the usual manner, over the entire rear surface of the cell. Then an insulating material is used to cover a cell edge and the desired part of the base contact. For the conventional N/P cell the N contact is then placed upon this insulated area and extends to the grids on the cell's active surface. With this configuration no P contact region is lost, and depending on the insulation coverage, the N contact can be placed anywhere on the back surface that could be required by specific array fabrication requirements.

A. Effect of Back Contact Removal

Previous work done by Heliotek using the etched wraparound junction design showed that the loss of some of the base (P type) contact resulted in an increase in the current path through the bulk silicon. This increased the series resistance, leading to a reduction in power output and efficiency. In order to accurately determine the limitations caused by this effect an experimental program to study power output and series resistance as a function of P contact area loss was initiated. Two different contact removal configurations were examined: 1) removing contact area from one edge, and 2) removing contact area from the center of the cell. Four test samples were used for each sequence. First 2 x 2 cm cells with a conventional front bar contact and total rather than picture frame back contacts were measured electrically to determine the maximum power output as well as the series resistance.

The measurement of series resistance employed the two light level technique.⁽³⁾ This method requires that the I-V curve of the cell be measured at two different light levels that need not be known. This can be done because for a finite amount of internal resistance there will be a shift in voltage at any point on the curve equivalent to IR_s where I is the current at that particular point. Coupling this shift with the shift in current caused by a different light level allows a solution for R_s to be obtained. In practice an arbitrary interval is chosen on the current axis corresponding to $I_{sc} - \Delta I$, and this same ΔI is used to locate the second current point for the other light level, $I'_{sc} - \Delta I$. The interval chosen should be such that the new point on the I-V curve is close to the maximum power point. By connecting these points on the two different light level curves, the series resistance, which is the slope of that straight line can be calculated.

After determination of R_s the cells were masked and measured amounts of the back (P type) contact were removed by etching. When contact area was removed from the edge, that edge opposite the front ohmic bar was selected since the test fixture probe for the base (back) contact was located near the edge beneath the front collector bar. After each etch the cells were measured again to determine the new maximum power point and series resistance. A control cell was used to verify the illumination intensity before each set of measurements. Increments up to 63 percent of the back contact area were removed in this test sequence. Results of this experiment are presented in Figures 1 and 2 for the case of edge and center contact removal.

Series resistance in a solar cell is the result of many elements such as contact resistance, diffused region thickness, contact material and geometry as well as the amount of back contact coverage. In the latter case the bulk resistance enters into our consideration since the minority carriers must traverse this relatively high resistance region before being collected at the contact.

An increase in series resistance results in a loss of cell fill factor ($V_{mp} I_{mp}/V_{oc} I_{sc}$). The short circuit current and open circuit voltage are unchanged for values of series resistance up to a few ohms, but the current and voltage at maximum power are reduced.

This work indicated that between 10 and 15 percent of the P contact area could be removed without seriously reducing the power output. Beyond this there was a sharp reduction in power which was more extreme in the case of removal of contact from the edge. This effect is explained by considering the path length from the etched region to the remaining contact area. In the case of edge contact removal the path length increases directly as a function of area removed; for center removal the path length increases only one half as rapidly resulting in a smaller increase in series resistance.

The series resistance curve shapes for both cases are in general agreement. Ten to fifteen percent contact removal has little effect on the cell's total series resistance; beyond this there is a transition region where series resistance increases sharply and finally a region where series resistance monotonically increases with increasing back contact removal. This experiment indicates that at least ten percent of the back contact can be removed with only a one or two percent loss in cell output power.

B. Insulated Wraparound Contact

As a parallel effort Heliotek undertook a brief examination of techniques for producing insulated wraparound contacts. For successful insulation the choice of materials is governed by a variety of requirements. The material must be adherent to silicon and the contact material must be adherent to it. It must have good dielectric strength and must be capable of being deposited in thin, pinhole-free layers. In addition the insulator must be capable of surviving the typical contact sintering temperatures used for solar cells. It should be compatible with standard masking techniques, be capable of giving good edge coverage and be humidity resistant.

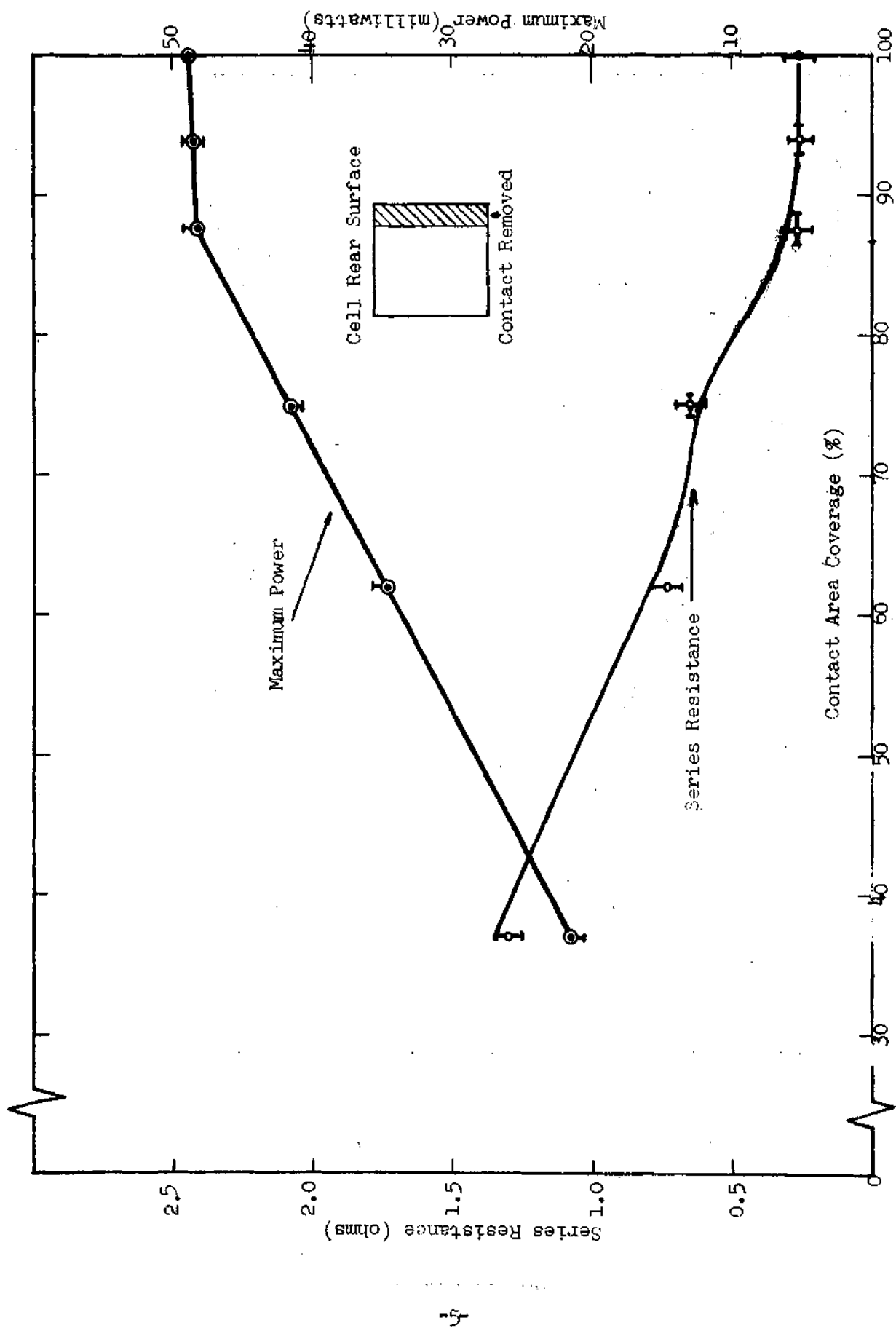


Figure 1. Effect of Edge Strip Removal on Cell Series Resistance and Maximum Power

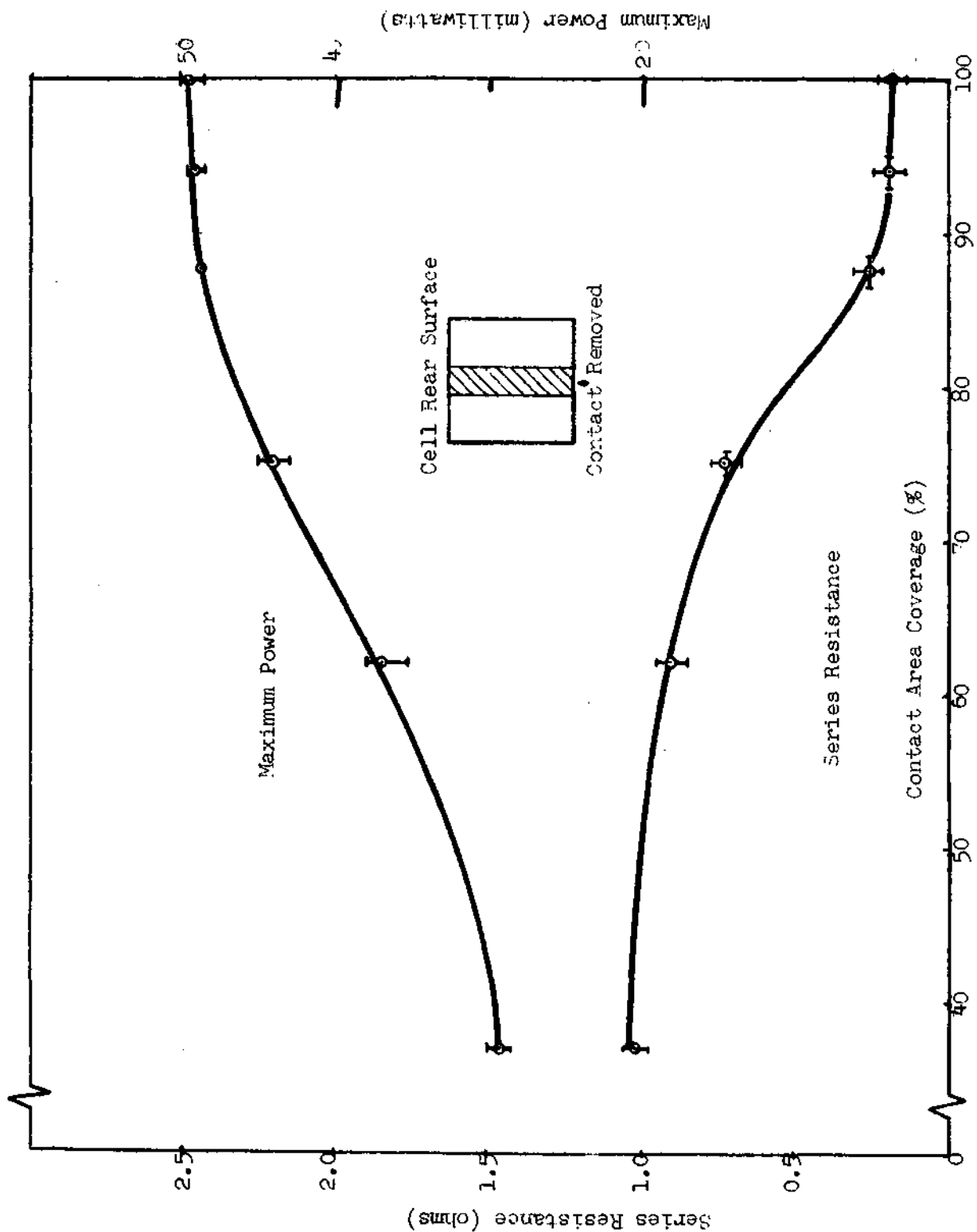


Figure 2. Effect of Center Strip Removal on Cell Series Resistance and Maximum Power

A thin film dielectric material deposited by evaporation techniques could be employed and therefore a number of dielectrics were investigated. The most likely candidates were silicon monoxide (SiO), titanium dioxide (TiO_2), silicon dioxide (SiO_2), aluminum oxide (Al_2O_3) and glass. The first two materials are commonly used for antireflection coatings while the other three had been used at Heliotek on other programs.

Initially SiO was examined since it is used on conventional solar cells. Multiple quarter wave length coatings were deposited onto the back⁽⁴⁾ contact of cells and tested for adherence using the standard erasure test. These films failed to survive abrasion tests as was the case with TiO_2 . Post deposition heat treatments did not improve the adherence in either case.

Corning Glassworks #1720 glass was examined as an insulator since we had a great deal of experience in employing the material as an integral cover for solar cells. Films of $\sim 25 \mu\text{M}$ were deposited onto solar cell Ag-Ti contacts using electron beam evaporation techniques. The coatings were hard and adherent. Typical evaporation parameters were a condensation rate of 200 $\text{\AA}/\text{sec}$, source power of 2 kw, and a substrate temperature of 250-300°C.

Standard silver-titanium contacts were deposited onto the glass coated cells and these structures were tested for adherence. In all cases the contacts could be removed by standard tape peel tests thus eliminating this type of glass from consideration.

Two other dielectrics, aluminum oxide (Al_2O_3) and silicon dioxide (SiO_2) were investigated. Both materials are abrasion resistant and can be uniformly deposited by electron beam evaporation. To avoid problems caused by the surface finish of typical etched-back silicon cells, the blanks were chemically polished before contacting. Aluminum rather than silver-titanium was used as a contact for convenience. A number of depositions upon aluminum using both Al_2O_3 and SiO_2 were performed and the evaporation parameters are given in Table 1.

Each sample was given a tape peel test, subjected to a water boil for one hour, then erased using the standard abrasion test. Both Al_2O_3 and SiO_2 coatings passed these tests and were used in the next evaluation² phase. Al_2O_3 and SiO_2 were evaporated onto aluminum coated silicon wafers and a second layer of aluminum was evaporated upon the dielectrics in order to form a rudimentary capacitor sandwich. The structures were tested to ensure a satisfactory metal to dielectric bond and they successfully passed both water boil and tape peel tests.

By measuring these sandwiches as capacitors we could evaluate their isolating properties in a quantitative manner. In all cases, even for 8 μM thick, SiO_2 , the capacitor sandwiches were shorted, which indicated pinholes in the dielectric. Examination of the dielectric showed that defects such as etch pits and high spots in the silicon caused the insulator to fail at that point.

To overcome this problem attempts were made to deposit thicker films of both materials. Silicon dioxide layers in excess of 15 μM resulted in satisfactory electrical isolation. This was verified by depositing a small

Table 1

Evaporation Parameters for Thin Film Insulators

Material	Source Power (kw)	Deposition Rate ($\text{\AA}/\text{sec.}$)	Thickness (μM)
Al_2O_3	0.60	2	0.25
Al_2O_3	0.60	10	0.25
Al_2O_3	0.60	15	0.40
Al_2O_3	0.60	20	0.60
Al_2O_3	0.60	10	1.5
Al_2O_3	0.60	15	2.5
Al_2O_3	0.60	30	5.0
Al_2O_3	1.2	160	30
SiO_2	0.18	20	1.2
SiO_2	0.18	40	2.5
SiO_2	0.18	75	4.4
SiO_2	0.30	170	8.0
SiO_2	0.3	260	16
SiO_2	0.3	300	18

square of Al upon the SiO₂ covering a typical Ag-Ti back etched contact and then measuring this structure as a capacitor. Measurements gave a dielectric constant (3.7) close to published values for SiO₂ (~4.0). The dielectric strength was approximately 3×10^4 volts/cm for our better SiO₂ films. No information about the dissipation factor was obtained, but the low value of dielectric strength suggested that these films were far from optimum. Similar efforts were taken using Al₂O₃, but this material displayed poor adherence at thicknesses greater than 5 μ m.

Since the program schedule required a decision concerning the wrap-around contact design within a relatively short time it was concluded that on the basis of the work done in investigating dielectric insulation it would be prudent to select the etched contact wraparound design for the manufacturing phase.

The insulated wraparound contact work pointed out several areas of research that must be undertaken before this technique is suitable for large scale production. Although at least two candidates, Al₂O₃ and SiO₂ showed promise it will be necessary to thoroughly investigate the pertinent evaporation parameters that control the reproducibility of the depositions. Even more important it will be necessary to prepare the surface of the silicon blank so that a smoother finish results. Conventional cells have a surface finish between 300 and 400 nm rms. For a pinhole-free film the finish may have to be below 25 nm rms. To achieve this will require additional material preparation steps as well as some modification in the present techniques for back etching silicon.

In addition to the surface finish criterion there is the question of deposition method. In general the properties of evaporated materials are a strong function of the angle of incidence. To obtain a condition where both the wraparound edge and the back of the cell are insulated with dielectric possessing identical mechanical properties will require rotisserie tooling or two separate evaporations. In either case the present techniques for depositing dielectrics require extremely sophisticated equipment and added processing steps which will increase the cost of the cell.

C. Wraparound Junction Contact

Because the insulation technique for wraparound contacts could not be reduced to practice within the time allowed, it was necessary to use the etched wraparound design. The configuration which is shown in Figure 3 was chosen on the basis of reliability and ease of fabrication. The front contact has six grid lines which are flared slightly as they approach the cell edge in order to provide added mechanical strength for the wraparound portion of the grids. To assure a reliable edge contact the grid lines join a metal film evaporated onto the cell edge. This acts as a carrier for the grid lines to wrap them around to the back. The terminating ohmic bar for the front contact is thus located on the back of the cell yielding an increased active cell surface area.

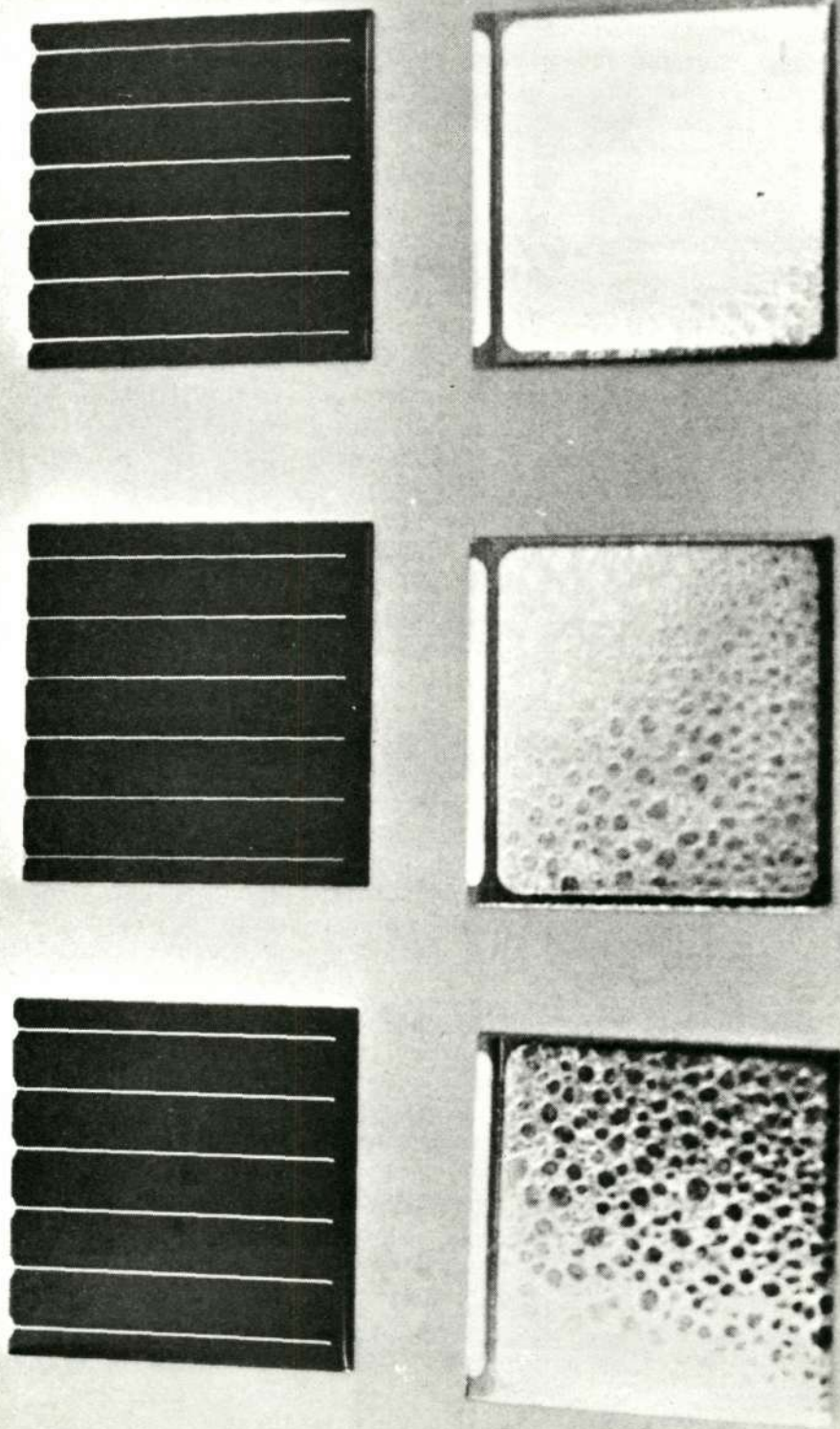


Figure 3. Wraparound Contact Solar Cells

The back contact design was a compromise between tooling capability and our study of output power as a function of P-contact coverage. This configuration, with dimensions, is given in Figure 4. It consists of an N-type collector bar contact separated from the Heliotek standard picture frame P-type contact by an etched isolation region. The isolation region was etched so that the portion next to the collector bar was N-type and the portion bordering the picture frame contact was P-type.

The P-type contact comprises 82.5 percent of the cell's back surface. Reference to Figure 1 shows that this configuration will cause a reduction in output power of approximately four percent. It was our judgment that increasing the P-type contact area by reducing the isolation region or picture frame border would have severely reduced the yield of 10.5 percent efficient cells. This is not to imply that such an approach would not be practical, but cost and scheduling constraints on this particular contract precluded this from being attempted.

IV. CELL FABRICATION

A. Blank Preparation

Figure 5 shows the processing sequence used to obtain the 10 ohm cm wraparound cell blanks. The normal process for producing silicon slices is to section the ingot into slabs and cut $\sim 2 \times 2$ cm slices from these slabs using a wire saw with a silicon carbide abrasive. These slices are then chemically polished to the proper dimensions in order to remove the mechanical damage caused by cutting. Since the cell edge corresponds to that region cut in sectioning, it possesses blade marks which are sensitive to chips and nicks in handling.

A conventional cell is relatively unaffected by edge nicks and chips, but in the case of a cell where the junction wraps around to the back, these defects reveal P-type (bulk) material, which when covered with metal causes shunting. Figure 6 shows an extreme example of edge damage caused by this processing sequence.

Cells were made using conventionally prepared blanks and Figure 7₂ shows the type of I-V curve which resulted. AMO efficiencies (135.3 mW/cm^2) between 9.5 and 10.5 percent were obtained; the low values were mainly caused by poor curve shape attributable to shunting.

To solve this problem the silicon slab faces were mechanically lapped to remove saw marks before slicing. It should be noted that the final operation of chemically polishing the wafers gives a rounded edge to the cell which we found to be necessary in order to avoid breaks in the metallized wraparound contacts.

B. Diffusion

In order to minimize edge chips during processing new handling procedures were instituted. Before diffusion the blanks were examined and a particular edge was selected as the wraparound edge. The blanks were mounted in the diffusion boat with this edge in the "up" position. Usually after a

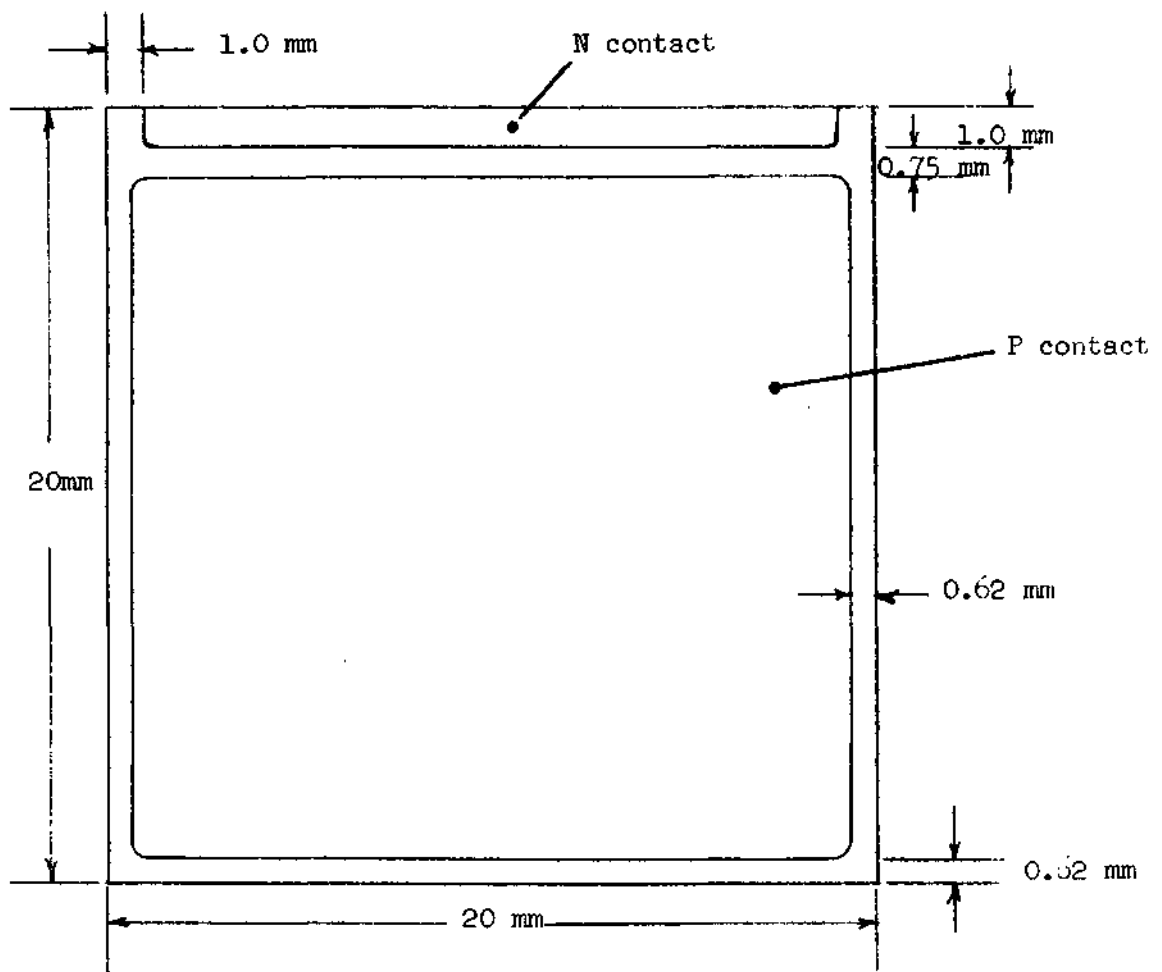


Figure 4. Back Contact Design

WAFER PREPARATION

10 Ω -cm. P-type Silicon Ingot

Section



2.1 \times 2.1 \times 2.0 cm. SLAB

Lap Faces and Slice



2.03 \times 2.03 \times 0.045 cm. Wafer

Chemical Etch



2.0 \times 2.0 \times 0.033 cm. Blank

Figure 5. Wafer Preparation Flow Chart

Reproduced from
best available copy.

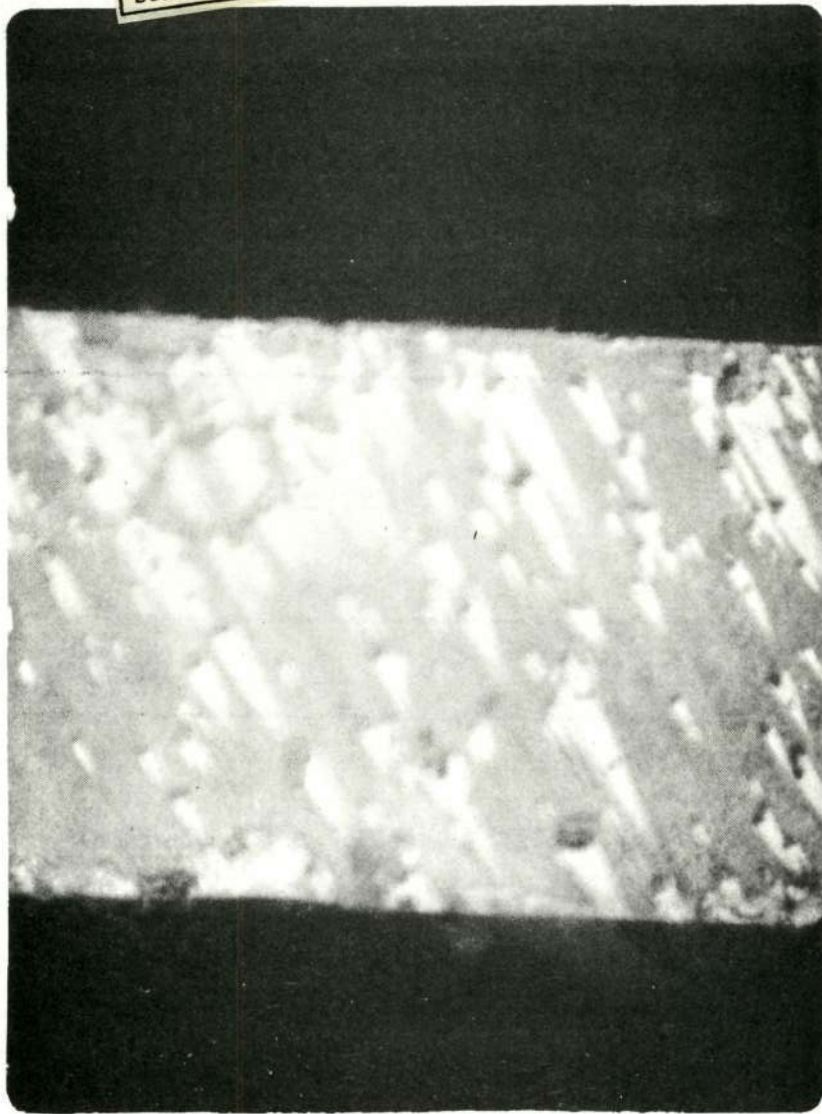


Figure 6. Cell Edge Damage

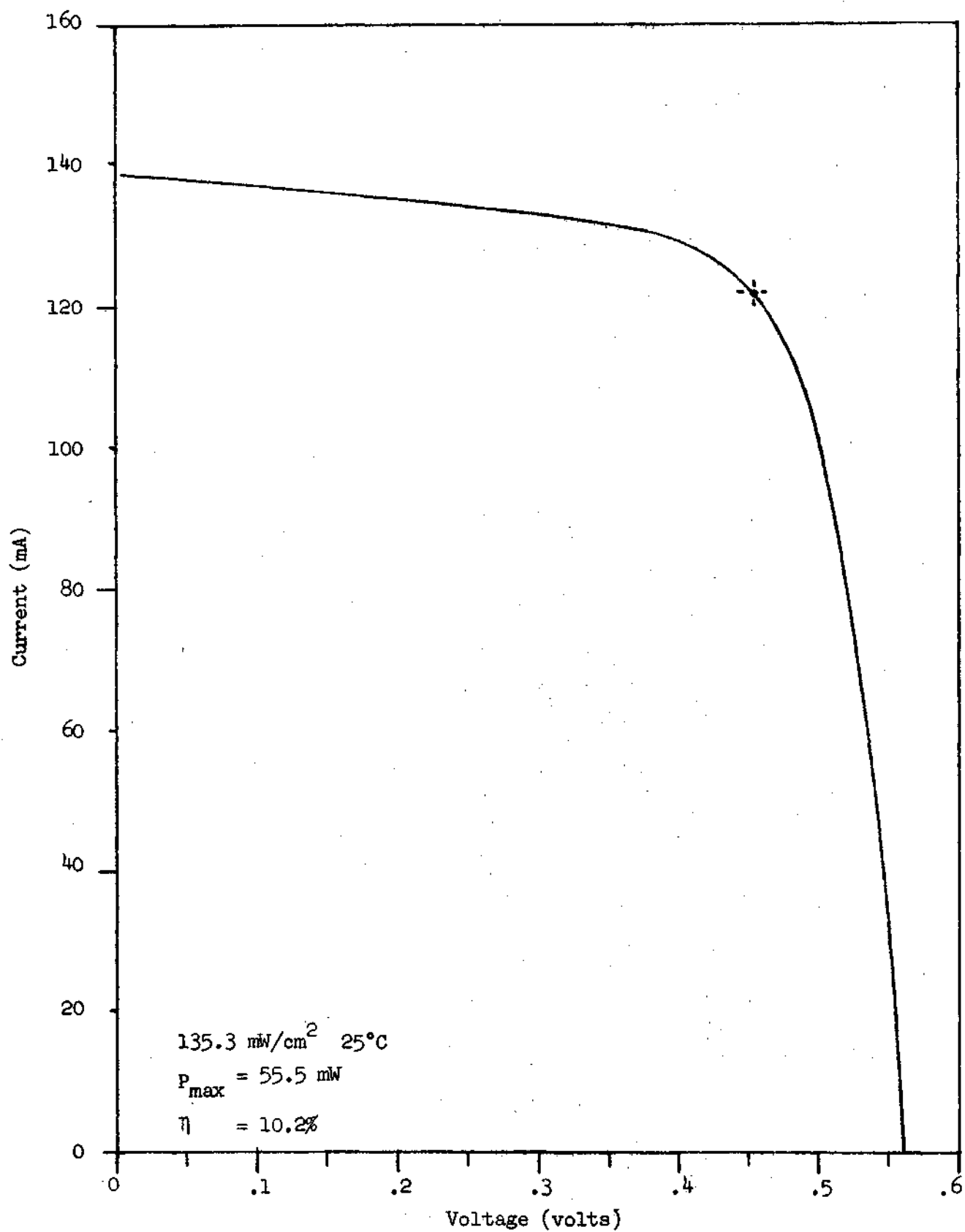


Figure 7. Initial Wraparound Cell (Conventional Processing)

diffusion the blanks will adhere slightly to the slots in the quartz diffusion boat and in removing them there is some chance that edge chips may be created. If that edge were used for the wraparound there would be a high probability of forming a shorted region when the edge was metallized. A second potential problem that was eliminated concerned the junction region. The cell edge that is down in the slot may possess a slightly shallower junction since it is partially shielded from the diffusant and this would make it more sensitive to contact punch-through during sintering. After diffusion the cells were transferred to slotted boxes with the pre-selected edge in the "up" position in order to retain edge identity.

A change was made in the diffusion schedule. Since the initial cells fabricated by conventional processing had high leakage (dark reverse) currents ($>1 \text{ mA/cm}^2$ at $V_R = 0.7\text{V}$) we investigated diffusion depth as a function of output power, reasoning that a slightly deeper junction would give a better curve shape by reducing the incidence of shunting which causes high dark reverse leakage currents, more than compensating for any reduction in short circuit current. A series of standard phosphorous diffusions using a gaseous source were made in which all the parameters except diffusion time were held constant. It was found that a 20 minute diffusion at 900°C yielded wraparound cells with improved curve shape. Cells made using the modified diffusion schedule had AMO efficiencies in excess of the 10.5 percent required.

Dark reverse current measurements of these cells indicated leakage currents as low as $1\text{-}2 \text{ }\mu\text{A/cm}^2$ with the majority of cells showing reverse leakage currents between $10\text{-}30 \text{ }\mu\text{A/cm}^2$ ($V_R = 0.7\text{V}$). A more thorough evaluation of output as a function of leakage current will be made in a later section.

C. Masking and Etching

The diffused blanks were cleaned with dilute HF and rinsed with water and alcohol before being masked for etching. The masking was done by applying an organic protective coating sequentially to three specific areas of the cell. The front surface was masked first, then the pre-selected wrap-around edge was coated. Following this a 1.4 mm wide strip on the back of the cell was masked. The cells were then etched in an HF-HNO_3 mixture to remove the n region from the rear surface. After rinsing the cells were ready for contacting.

D. Contacts

The standard silver-titanium contacts were evaporated using resistive heating techniques. It was necessary to evaporate the edge contact in a separate run to prevent poor adherence. Evidently the silver adherence is sensitive to the incidence angle and therefore normal incidence evaporation had to be employed. The cells, separated by specially machined aluminum spacers, were mounted in a metal box for this deposition. (See Figure 8). The spacers were designed so that a knife edge configuration was obtained in order to prevent metal overspray both to the front and back surface of the cell. The initial spacer design failed to achieve this situation and the metal overspray caused contact failure when tape tested.

After the edge contact was deposited the cells were removed from the vacuum system and loaded into evaporation masks for front and rear contacting. Figure 9 shows the masks used for this operation. The active area contact

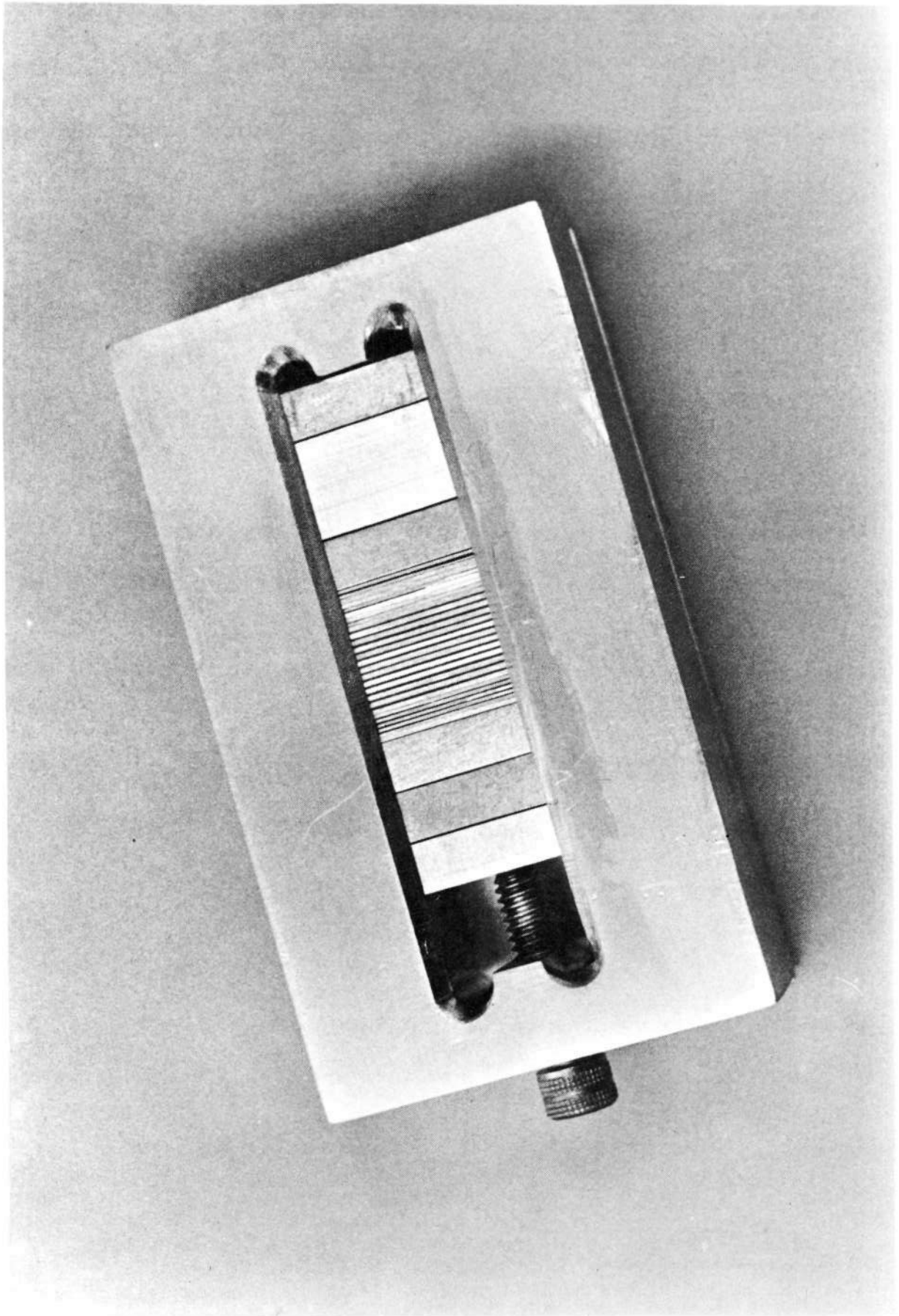


Figure 8. Edge Evaporation Tooling

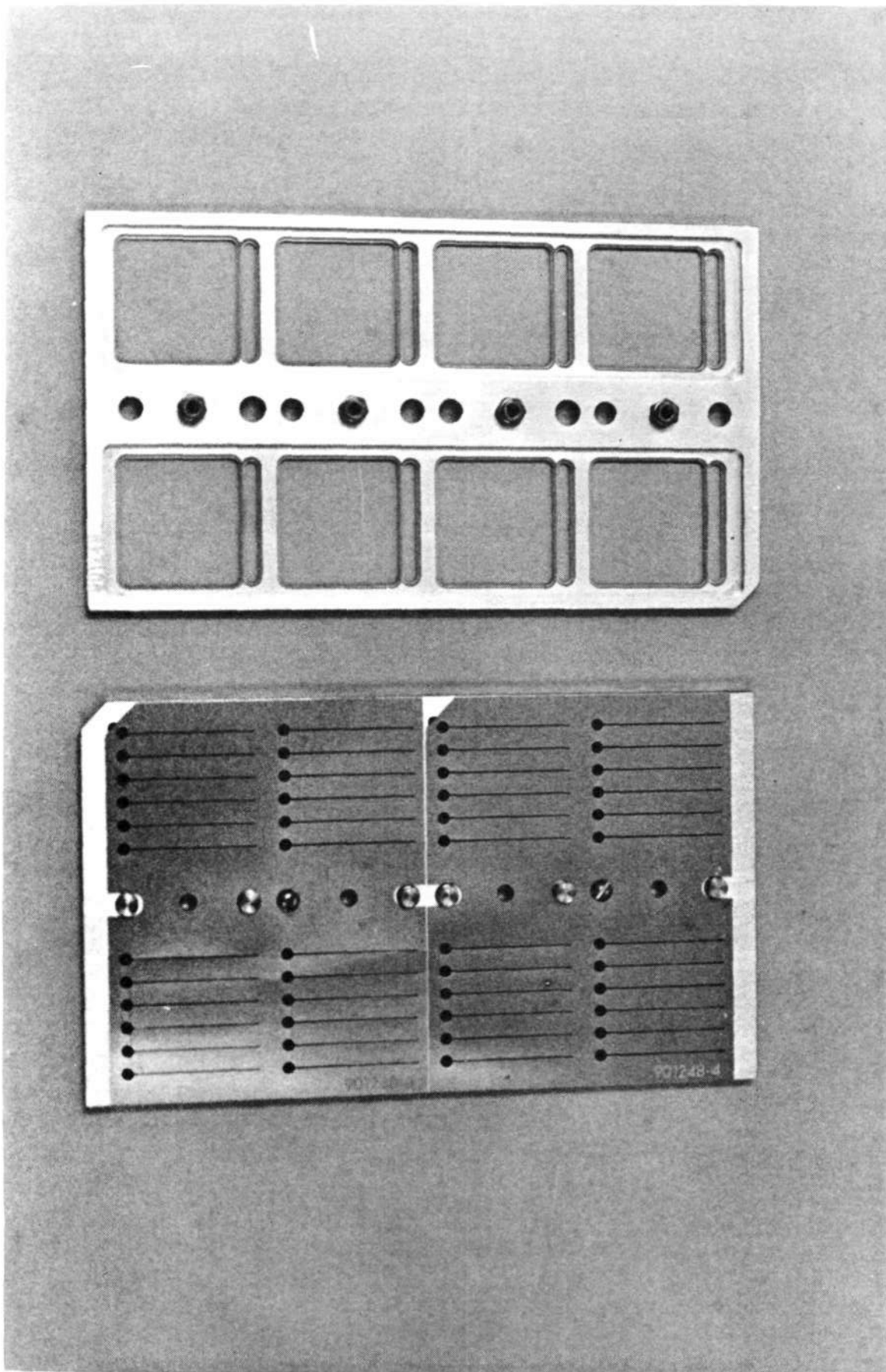


Figure 9. Contact Masks

had six grid lines extending to connect to the edge contact. The grids were deliberately flared at the ends to give added mechanical strength. Initially the standard Heliotek tapered grid lines whose effective width was .020 mm were used. New grid line masks were fabricated with both 0.15 mm and 0.10 mm wide grid lines in order to increase the active area, thus regaining any current lost by employing the slightly deeper diffusion. Cells meeting the efficiency specifications of this program were obtained using both types of grids. It was noted that cells with the thinner grids (0.10 mm) possessed more series resistance and did not therefore outperform the wider grid line (0.15 mm) cell.

The back contact mask used a 0.75 mm wide bar to form an isolation region composed of equal areas of unmetallized p and n-type silicon. This strip acted as a buffer against any accidental overspray of metal from either the wraparound or the bulk region contact.

E. Sintering and Antireflection Coating

The cells were cleaned, rinsed and spun dry, then coated with silicon monoxide using standard deposition techniques. Following this procedure they were sintered in a reducing atmosphere at $\sim 600^{\circ}\text{C}$ for a few minutes.

V. TESTING AND EVALUATION

A. Mechanical Integrity

Each cell was tape tested to ensure contact integrity. The wraparound contact was tested by pressing the wraparound edge securely to a strip of #810 Scotch Brand tape and peeling it away. In some cases small amounts of metal corresponding to grid line overspray came free. This is not unexpected since the adherence of silver is sensitive to angle of incidence. These particular cells were cleaned and given a second tape peel test. If no additional metal came free the cells proceeded to electrical testing.

Statistics were kept for edge contact integrity and the yield at this point was in excess of eighty percent with the majority of the failed cells occurring during the initial phase of the production run. Edge contact failures generally were concentrated in specific lots, indicative of a processing variation in that lot rather than a general problem. A lot consisted of 24 cells and better than sixty percent of the lots had no edge contact failures.

B. Electrical Test

A special test fixture was designed for the wraparound cells. A vacuum hold-down was employed with a pair of spring loaded metal fingers making contact to the wraparound contact when the fixture was in the test mode. The cells were measured at $25 \pm 2^{\circ}\text{C}$ under an AMO illumination spectrum corresponding to 135.3 mW/cm^2 supplied either by a Spectrosun Model 1206 or Model X-25 solar simulator.

It was determined that the maximum power point was at 445 mV in almost all cases. To obtain a minimum efficiency of 10.5 percent based on an active area of 4.0 cm^2 the current at this point had to be 127.7 mA. The cells were tested at 445 mV and graded in 0.1 percent increments starting at 10.5 percent.

Five test lots totaling 1000 cells with AMO efficiencies of at least 10.5 percent were obtained and delivered to NASA Lewis Research Center. Figure 10 is a bar graph of the efficiency distribution of the delivered cells. Over half of these cells had 11.0 percent or higher AMO efficiencies. The short circuit current of these cells ranged from 140 to 155 mA (see Figure 11) while open circuit voltages were between 530 and 570 mV. The wide variation in open circuit voltage was caused by difficulties in the contact evaporation process which arose during the first part of the program. This problem was corrected and the open circuit voltages of the last 500 cells delivered was between 550 and 570 mV. Representative curves of delivered cells are shown in Figures 12 through 14.

Typical conventional 2 x 2 cm 10 ohm-cm cells of this thickness will have a short circuit current ranging from 137 to 143 mA. Since removing the collector bar from the front surface adds approximately five percent to the active area, the expected value of I_{sc} would be between 144 and 150 mA. Since three different grid line widths were used during the program as well as a slightly deeper diffusion the wider variation in short circuit current is easily explained.

C. Series Resistance

Cells from each test lot were randomly selected and series resistance measurements were made using the two light level technique. It was found that the series resistance of the wraparound cells varied from 0.40 to 0.60 ohm. Our study of series resistance as a function of rear surface contact area (Figure 1) indicates a value of 0.4-0.45 ohms for the configuration used for this cell (82.5% coverage). Some possible explanations for the higher series resistance values we observed are given in Section VI of this report.

D. Shunt Resistance

In the initial phases of this contract high leakage currents related to edge chips caused poor curve shapes. With the introduction of improved handling techniques as well as a slight change in junction depth this problem was solved. Present wraparound cells can tolerate leakage currents up to 1 mA/cm², as was demonstrated by the following test. Sixty-six wraparound cells each 10.8 percent efficient had dark reverse currents measured at 0.7V. The leakage currents varied from 1×10^{-3} to 1×10^{-6} A/cm² with the majority having currents below 100 μ A/cm². Although no correlation can be seen between leakage current and efficiency, it is interesting to note that twenty cells all having an AMO efficiency of 11.2 percent had leakage currents between 5×10^{-4} to 1×10^{-6} A/cm² with the majority below 20 μ A/cm². From this we conclude that leakage currents have only a secondary effect on wraparound cell efficiency provided that they are kept below 1 mA/cm².

VI. DISCUSSION

This program has demonstrated that wraparound contact cells can be fabricated using basic manufacturing processes. Although the efficiency requirement was achieved it must be admitted that the full benefits of the wraparound cell have not been realized during this program. Our experimental work has clearly identified back contact area as the key obstacle to full realization of the increased output power that wraparound cells can deliver. Any junction

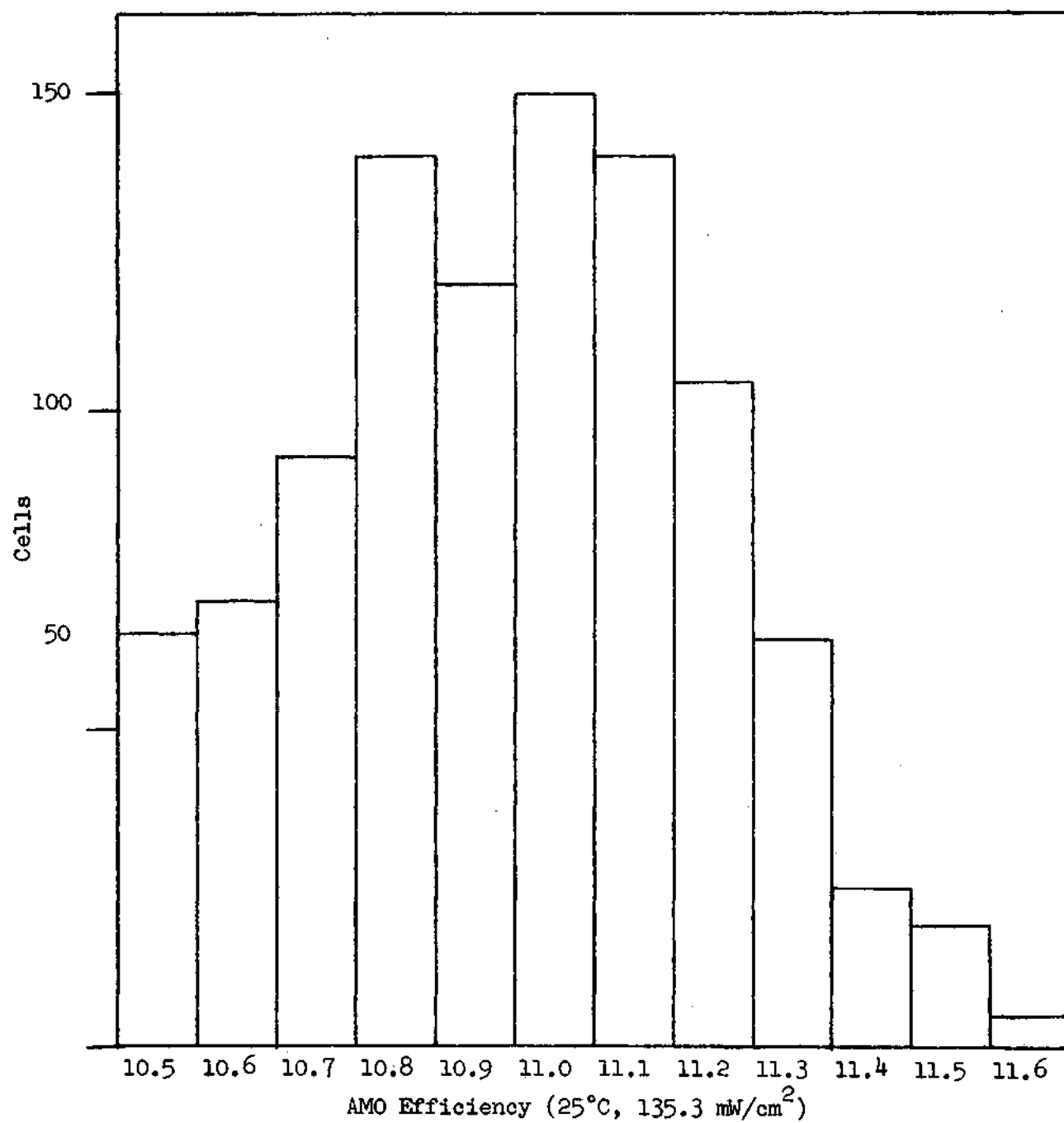


Figure 10. Efficiency Distribution for Wraparound Cells

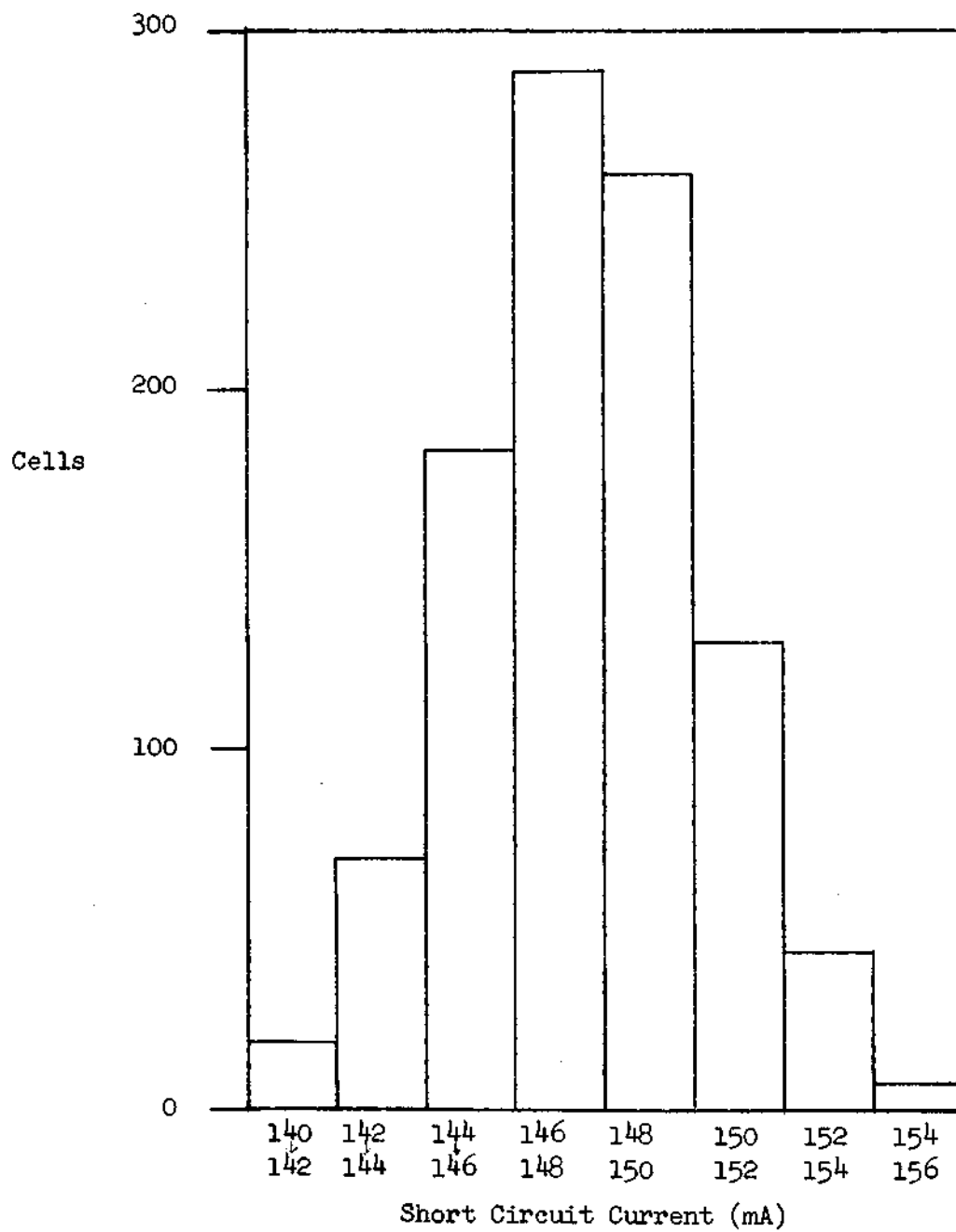


Figure 11. Short Circuit Current Distribution for Wraparound Cells

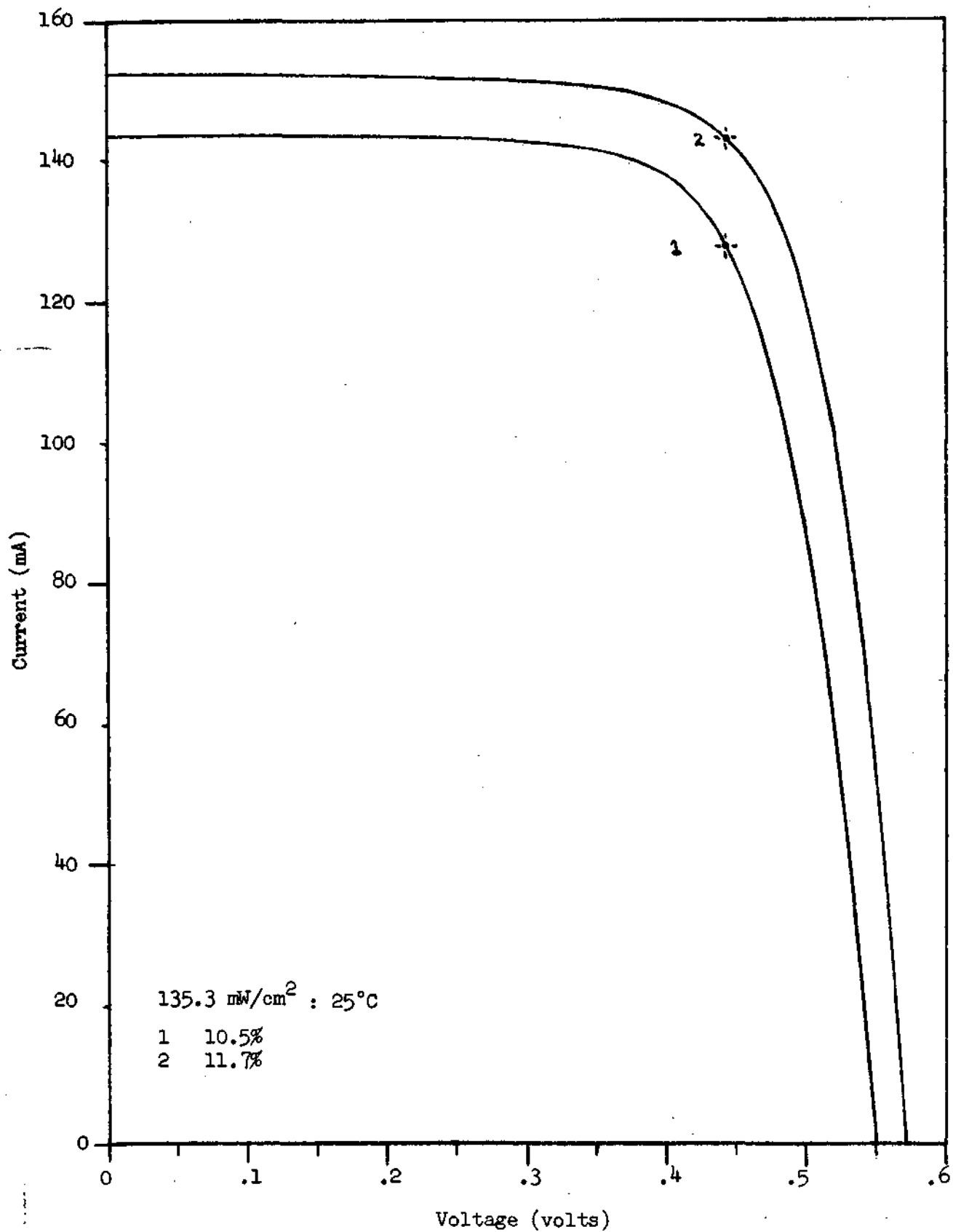


Figure 12. I-V Curves Showing Efficiency Extremes for Wraparound Cells

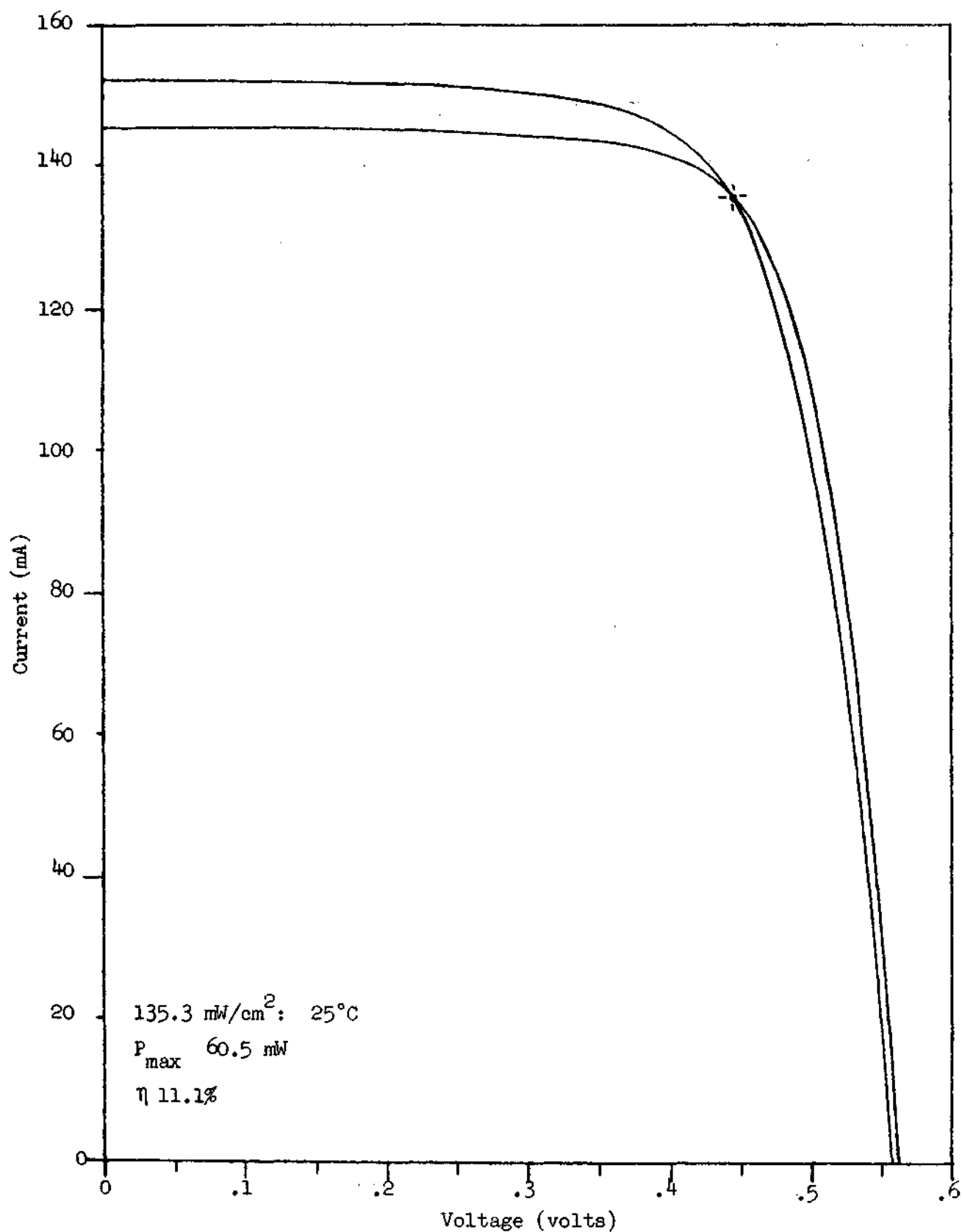


Figure 13. I-V Curves of Representative Wraparound Cells (I)

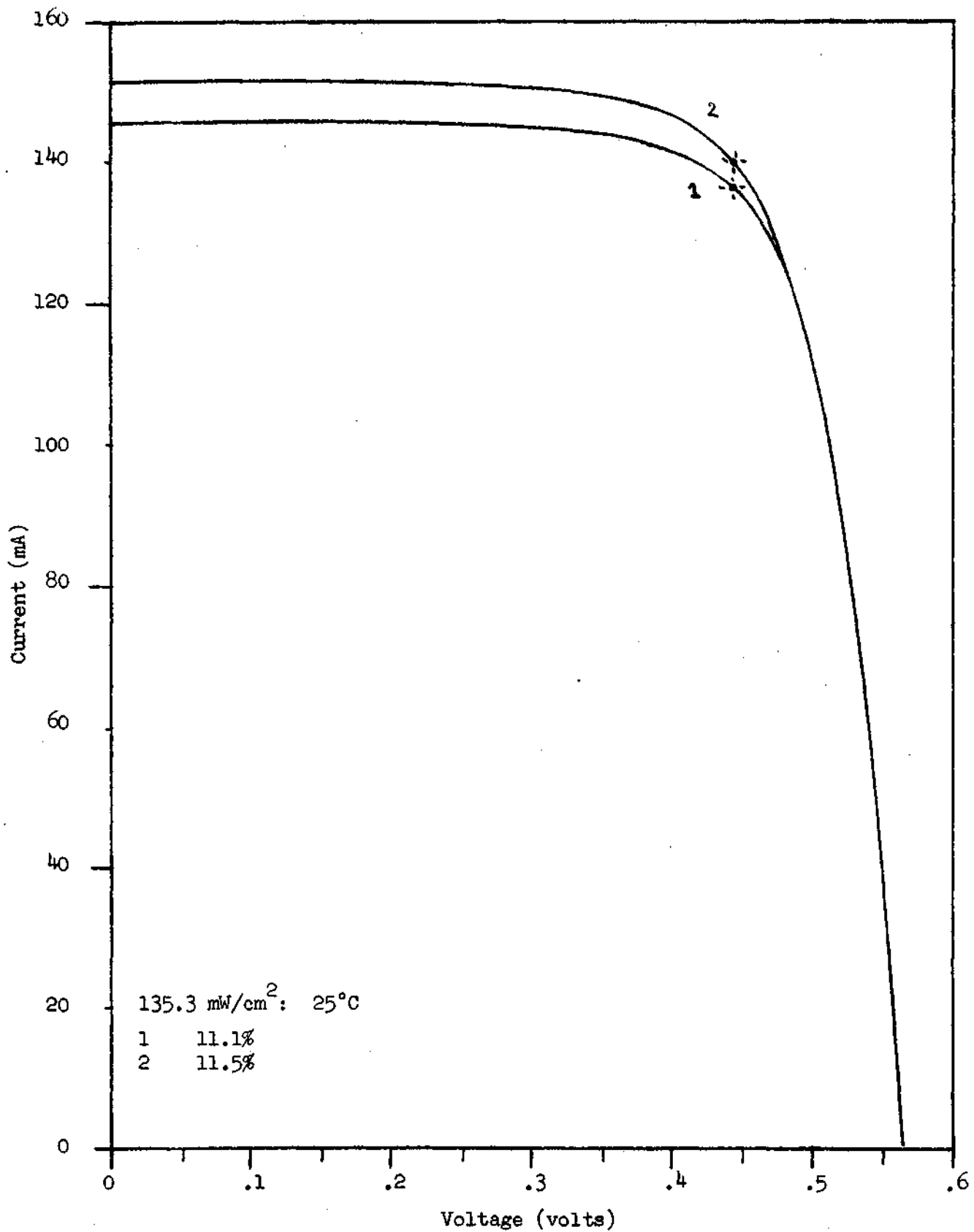


Figure 14. I-V Curves of Representative Wraparound Cells (II)

wraparound device causes some increase in series resistance since bulk contact area must be sacrificed. We feel that it is possible to design more complicated contact configurations that would allow up to ninety percent of the cell back surface to be used as the base contact. If this were achieved, power losses due to increased series resistance could be reduced to approximately two percent. Since there should be a gain of five percent in active area due to the elimination of the front surface collector bar, the net gain in power would be about three percent over conventional cells.

As described in section IV-D the wraparound cell contact configuration required two separate pumpdowns. From an economic aspect this is not an efficient process since a significant amount of time is lost while the cells are cooling after each evaporation. There is a great deal of labor involved in loading and then reloading cells for the second evaporation. There is also an element of risk involved in exposing cells to the environment after they have been originally cleaned for contacting.

A logical solution to the contact processing step would be to rotate the cells during evaporation using rotisserie tooling. This would eliminate the need for a second evaporation thus preventing possible contamination of the silicon surfaces, and allow normal incidence evaporations to be made on the edge and the corners, eliminating any variation in metallization thickness. Unfortunately the scope of this program precluded the investment of time and funding that would be necessary to install such equipment.

The insulated wraparound would allow full utilization of the back contact, but a number of problems remain unsolved at this point. Basically the work showed two major obstacles for insulation; 1) silicon surface finish and 2) physical defects (pinholes) in the dielectrics. These forced us to resort to unrealistic deposition thicknesses. The surface finish necessary for good dielectric isolation (25 nm rms) is well below that obtained using normal manufacturing procedures (300-400 nm rms). To get to this level would require a major change in wafer preparation, such as lapping each blank before chemical polishing, and a change in the technique for removing the diffused region from the rear surface of the cell. Both steps would have an adverse effect upon cost. Another problem that must be faced is developing the processing techniques for reliably depositing the dielectric. This will require much more sophisticated equipment and a higher level of operator skill than is generally expected in a manufacturing environment. This will add to the labor cost of the finished cell.

The wraparound junction method requires that the cell have a rounded edge to ensure the mechanical integrity of the wraparound contact metallization. Fortunately the final wafer preparation step involves chemically polishing the silicon which creates the desired edge contour. The rounded edge also acts to reduce chips and nicks in handling. As mentioned previously these edge imperfections caused significant shunting in the cell and the situation was corrected by instituting new handling procedures especially in blank grading and diffusion. Since these efforts have significantly reduced the influence of shunting, the problem of series resistance now assumes the dominant role in determining output power.

Experimentally it has been demonstrated that for the bulk contact coverage of our wraparound configuration the series resistance should be 0.4-0.45 ohm. By contrast the series resistance of a properly fabricated conventional cell is between 0.2 and 0.3 ohm. A random sampling of cells shows values of series resistance between 0.4 and 0.6 ohm. The fact that some number of wraparound cells show good agreement with our experimental work on back coverage as a function of series resistance indicates there are other factors which increase the series resistance of wraparound cells.

It is reasonable to suggest that variation in contact metal thickness was the main cause for the greater than predicted range of series resistance in the wraparound cells. The wraparound cells were "passengers" on large scale production line evaporation runs. Since the location of these cells in the evaporation pattern was not always the same it is quite possible that there could be some variation in the contact metal deposited from run to run. Another variable is the fact that there were two distinct grid line widths used, 0.1 mm and 0.15 mm. A calculation of the impact of this change shows that the series resistance would increase by .03 ohm if .1 mm grid lines were substituted for .15 mm grid lines.

The cells manufactured for this program did yield about five percent more short circuit current than conventional cells because of the added active area, but a large fraction of this gain was not transferred to the maximum power point because of additional series resistance which resulted from the loss of back contact area as well as the techniques used for cell fabrication. Although the deeper junction did not have an impact on current because of grid line width reduction it must be admitted that this trade-off was only possible because conventional cells do not have optimized grid geometry. Comparing the two cell types with equivalent grid patterns indicates that wraparound junction cells did not offer any great advantage in output power.

VII. RECOMMENDATIONS

From the results of this program we conclude that the wraparound junction contact places a limitation on the output power of wraparound solar cells. The insulated wraparound concept should allow complete utilization of the additional active area obtained by placing the collector on the rear surface. As was discussed in the previous section, the main problem areas have been defined. We would recommend a serious effort aimed at developing the technology for this approach. The program would concentrate on producing very thin pinhole-free dielectrics which could be deposited in a reliable manner.

However, if the junction wraparound technique is suitable because of the advantages offered to the array fabricator then we would recommend consideration of a program to develop the technology to fabricate thin (100 μM -150 μM) wraparound cells. Since thin silicon cells display better radiation performance and a wraparound cell allows complete front surface protection it would seem logical to have such a cell for missions that required very small changes in output power over the lifetime of the mission.

REFERENCES

- 1) Chapin D.M., Fuller C.S., and Pearson G.L.; J. Appl. Phys., 25, pp. 676-677; May 1954
- 2) Goodelle, G.S. Heliotek Internal Report (1966)
- 3) Wolf M., and Rauschenbach H.; Advanced Energy Conversion, 3, pp. 455-479 (1963)
- 4) MIL-C-675A Jan. (1964)